CLAIMS

What is claimed is:

1. A low power low voltage differential signaling (LVDS) driver comprises:

a load current source operably coupled to provide a load current;

a first input transistor having a gate, a drain, and a source, wherein the source of the first input transistor is coupled to the load current source, and wherein the gate of the first input transistor is operably coupled to receive a first leg of a differential input signal;

a second input transistor having a gate, a drain, and a source, wherein the source of the second input transistor is coupled to the load current source, and wherein the gate of the second input transistor is operably coupled to receive a second leg of the differential input signal, wherein the drains of the first and second input transistors provide an output of the low power LVDS driver;

a first switchable current source operably coupled to the drain of the first input transistor and to a power supply source, wherein, when enabled, the first switchable current source provides a first current to the drain of the second input transistor via at least one of a source termination and a load;

a second switchable current source operably coupled to the drain of the second input transistor and to the power supply source, wherein, when enabled, the second switchable current source provides a second current to the drain of the first input transistor via the at least one of the source termination and the load; and

switchable current source control module operably coupled to selectively enable the first and second switchable current sources based on states of the first and second legs of the differential input signal.

2. The low power LVDS driver of claim 1, wherein the first switchable current source comprises:

a first P-channel transistor having a gate, a drain and a source, wherein the gate of the first P-channel is operably coupled to receive a first gating signal from the switchable current source control module, the source of the first P-channel transistor is operably coupled to the power supply source, and the drain of the first P-channel transistor is operably coupled to the drain of the first input transistor, wherein, when the first gating signal is in a first state, the first switchable current source is enabled; and

a first active pull-up and pull-down circuit operably coupled to the gate of the first P-channel transistor to actively turn on and turn off the first P-channel transistor in accordance with the differential input signal and corresponding to the first gating signal.

3. The low power LVDS driver of claim 2, wherein the first active pull-up and pull-down circuit comprises:

a pull-up module including:

a first delay circuit operably coupled to delay the differential input signal to produce a first delayed signal;

first switching circuitry operably coupled to produce a first gate drive signal in accordance with the first delayed signal; and

a pull-up transistor operably coupled to pull-up a voltage of the gate of the first P-channel transistor based on the first gate drive signal; and

a pull-down module including:

a second delay circuit operably coupled to delay the differential signal to produce a second delayed signal;

second switching circuitry operably coupled to produce a second gate drive signal in accordance with the second delayed signal; and

a pull-down transistor operably coupled to pull-down a voltage of the gate of the first P-channel transistor based on the second gate drive signal.

4. The low power LVDS driver of claim 2, wherein the second switchable current source comprises:

a second P-channel transistor having a gate, a drain and a source, wherein the gate of the second P-channel is operably coupled to receive a second gating signal from the switchable current source control module, the source of the second P-channel transistor is operably coupled to the power supply source, and the drain of the second P-channel transistor is operably coupled to the drain of the second input transistor, wherein, when the second gating signal is in the first state, the second switchable current source is enabled; and

a second active pull-up and pull-down circuit operably coupled to the gate of the second P-channel transistor to actively turn on and turn off the second P-channel

transistor in accordance with the differential input signal and corresponding to the second gating signal.

5. The low power LVDS driver of claim 4, wherein the second active pull-up and pull-down circuit comprises:

a pull-up module including:

a first delay circuit operably coupled to delay the differential input signal to produce a first delayed signal;

first switching circuitry operably coupled to produce a first gate drive signal in accordance with the first delayed signal; and

a pull-up transistor operably coupled to pull-up a voltage of the gate of the second P-channel transistor based on the first gate drive signal; and

a pull-down module including:

a second delay circuit operably coupled to delay the differential input signal to produce a second delayed signal;

second switching circuitry operably coupled to produce a second gate drive signal in accordance with the second delayed signal; and

a pull-down transistor operably coupled to pull-down a voltage of the gate of the second P-channel transistor based on the second gate drive signal.

6. The low power LVDS driver of claim 1 further comprises:

a common mode voltage regulation circuit operably coupled to the drains of the first and second input transistors and to the load current source, wherein the common mode voltage regulation circuit:

senses a common mode voltage based on voltages on the drains of the first and second input transistors to produce a measured common mode voltage;

compares the measured common mode voltage to a reference voltage;

generates a control signal based on the comparison of the measured common mode voltage to the reference voltage; and

provides the control signal to the load current source to regulated the load current to maintain a desired common mode voltage level.

7. The low power LVDS driver of claim 6 further comprises:

the source termination including:

a first resistor having a first node and a second node, wherein the first node of the first resistor is operably coupled to the drain of the first input transistor; and

a second resistor having a first node and a second node, wherein the first node of the second resistor is operably coupled to the drain of the second input transistor and the second node of the first resistor is operably coupled to the second node of the second resistor to provide a common mode sense node; and

the common mode voltage regulation circuit including:

an amplifier having a first input, a second input, and an output, wherein the first input is operably coupled to receive the reference voltage and the second input is operably coupled to the common mode sense node, wherein the output of the amplifier provides the control signal.

8. The low power LVDS driver of claim 1, wherein the switchable current source control module comprises:

an adjustable current mirror circuit operably coupled to produce a reference current and a reference gate voltage;

a buffer operably coupled to buffer the reference gate voltage to produce a buffered gate voltage;

a first switch operable to couple the buffered gate voltage to the first switchable current source when the first leg of the differential input is in a first state; and

a second switch operable to couple the buffered gate voltage to the second switchable current source when the second leg of the differential input is in the first state.

9. An integrated circuit comprises:

circuitry operable to produce a plurality of data signals;

adjustable current mirror circuit operably coupled to produce a reference current and a reference gate voltage;

a buffer operably coupled to buffer the reference gate voltage to produce a buffered gate voltage; and

a plurality of low power low voltage differential signaling (LVDS) drivers, wherein each of the plurality of low power LVDS drivers includes:

a load current source operably coupled to provide a load current;

a first input transistor having a gate, a drain, and a source, wherein the source of the first input transistor is coupled to the load current source, and wherein the gate of the first input transistor is operably coupled to receive a first leg of a differential input signal that corresponds to one of the plurality of data signals;

a second input transistor having a gate, a drain, and a source, wherein the source of the second input transistor is coupled to the load current source, and wherein the gate of the second input transistor is operably coupled to receive a second leg of the differential input signal, wherein the drains of the first and second input transistors provide an LVDS output;

a first switchable current source operably coupled to the drain of the first input transistor and to a power supply source, wherein, when enabled, the first switchable current source provides a first current to the drain of the second input transistor via at least one of a source termination and a load;

a second switchable current source operably coupled to the drain of the second input transistor and to the power supply source, wherein, when enabled, the second switchable current source provides a second current to

the drain of the first input transistor via the at least one of the source termination and the load;

a first switch operable to couple the buffered gate voltage to the second switchable current source when the first leg of the differential input is in a first state such that the second switchable current source is enabled; and

a second switch operable to couple the buffered gate voltage to the first switchable current source when the second leg of the differential input is in the first state such that the first switchable current source is enabled.

10. The integrated circuit of claim 9, wherein the first switchable current source comprises:

a first P-channel transistor having a gate, a drain and a source, wherein the gate of the first P-channel is operably coupled to receive the buffered gate voltage via the first switch as a first gating signal, the source of the first P-channel transistor is operably coupled to the power supply source, and the drain of the first P-channel transistor is operably coupled to the drain of the first input transistor, wherein, when the first gating signal is in a second state, the first switchable current source is enabled; and

a first active pull-up and pull-down circuit operably coupled to the gate of the first P-channel transistor to actively turn on and turn off the first P-channel transistor in accordance with the differential input signal and corresponding to the buffered gate voltage.

11. The integrated circuit of claim 10, wherein the first active pull-up and pull-down circuit comprises:
a pull-up module including:

a first delay circuit operably coupled to delay the differential input signal to produce a first delayed signal;

first switching circuitry operably coupled to produce a first gate drive signal in accordance with the first delayed signal; and

a pull-up transistor operably coupled to pull-up a voltage of the gate of the first P-channel transistor based on the first gate drive signal; and

a pull-down module including:

a second delay circuit operably coupled to delay the differential input signal to produce a second delayed signal;

second switching circuitry operably coupled to produce a second gate drive signal in accordance with the second delayed signal; and

a pull-down transistor operably coupled to pull-down a voltage of the gate of the first P-channel transistor based on the second gate drive signal.

12. The integrated circuit of claim 10, wherein the second switchable current source comprises:

a second P-channel transistor having a gate, a drain and a source, wherein the gate of the second P-channel is operably coupled to receive the buffered gate voltage via the second

switch as a second gating signal, the source of the second P-channel transistor is operably coupled to the power supply source, and the drain of the second P-channel transistor is operably coupled to the drain of the second input transistor, wherein, when the second gating signal is in the first state, the second switchable current source is enabled; and

a second active pull-up and pull-down circuit operably coupled to the gate of the second P-channel transistor to actively turn on and turn off the second P-channel transistor in accordance with the differential input signal and corresponding to the buffered gate voltage.

13. The integrated circuit of claim 12, wherein the second active pull-up and pull-down circuit comprises:

a pull-up module including:

a first delay circuit operably coupled to delay the differential input signal to produce a first delayed signal;

first switching circuitry operably coupled to produce a first gate drive signal in accordance with the first delayed signal; and

a pull-up transistor operably coupled to pull-up a voltage of the gate of the second P-channel transistor based on the first gate drive signal; and

a pull-down module including:

a second delay circuit operably coupled to delay the differential input signal to produce a second delayed signal;

second switching circuitry operably coupled to produce a second gate drive signal in accordance with the second delayed signal; and

a pull-down transistor operably coupled to pull-down a voltage of the gate of the second P-channel transistor based on the second gate drive signal.

14. The integrated circuit of claim 9, wherein each of the plurality of low power LVDS drivers further comprises:

a common mode voltage regulation circuit operably coupled to the drains of the first and second input transistors and to the load current source, wherein the common mode voltage regulation circuit:

senses a common mode voltage based on voltages on the drains of the first and second input transistors to produce a measured common mode voltage;

compares the measured common mode voltage to a reference voltage;

generates a control signal based on the comparison of the measured common mode voltage to the reference voltage; and

provides the control signal to the load current source to regulate the load current to maintain a desired common mode voltage level.

15. The integrated circuit of claim 14 further comprises:

the source termination including:

a first resistor having a first node and a second node, wherein the first node of the first resistor is operably coupled to the drain of the first input transistor; and

a second resistor having a first node and a second node, wherein the first node of the second resistor is operably coupled to the drain of the second input transistor and the second node of the first resistor is operably coupled to the second node of the second resistor to provide a common mode sense node; and

the common mode voltage regulation circuit including:

an amplifier having a first input, a second input, and an output, wherein the first input is operably coupled to receive the reference voltage and the second input is operably coupled to the common mode sense node, wherein the output of the amplifier provides the control signal.

16. A low power low voltage differential signaling (LVDS) driver comprises:

switchable current module operably coupled to produce a first current when a differential input signal is in a first state and to produce a second current when the differential input signal is in a second state;

source termination circuit operably coupled in parallel with a load;

transistor section operably coupled to receive the first and second currents from the switchable current module via at least one of the source termination circuit and the load, wherein the transistor section produces an LVDS output signal based on the first and second currents, the differential input signal, and the source termination circuit; and

load current source operably coupled to sink the first and second currents from the transistor section.

17. The low power LVDS driver of claim 16, wherein the source termination circuit comprises:

a first resistor and a second resistor coupled in series, wherein a common node of the first and second resistors corresponds to a common mode voltage of the LVDS output signal.

18. The low power LVDS driver of claim 17 further comprises:

an amplifier having a first input, a second input, and an output, wherein the first input is operably coupled to receive a reference voltage and the second input is operably coupled to the common node of the first and second resistors, wherein the output of the amplifier provides a control signal to the load current source to regulate the load current such that common mode voltage of the LVDS output is maintained at a desired voltage level.

19. The low power LVDS driver of claim 16, wherein the switchable current module comprises:

a first transistor operably coupled to produce the first current based on a first gating signal;

a second transistor operably coupled to produce the second current based on a second gating signal; and

gating module operably coupled to produce the first and second gating signals based on the differential input signal and a reference gate voltage.

20. The low power LVDS driver of claim 19, wherein the gating module comprises:

an adjustable current mirror module operably coupled to produce the reference gate voltage;

a first switch operable to couple the reference gate voltage to a gate of the first transistor as the first gating signal when the differential input signal is in the first state; and

a second switch operable to couple the reference gate voltage to a gate of the second transistor as the second gating signal when the differential input signal is in the second state.

21. The low power LVDS driver of claim 19, wherein the switchable current module further comprises:

a first pull-up pull-down circuit operably coupled to the first transistor to actively turn on and turn off the first transistor in accordance with the first gating signal; and

a second pull-up pull-down circuit operably coupled to the second transistor to actively turn on and turn off the second transistor in accordance with the second gating signal.

22. The low power LVDS driver of claim 16, wherein the switchable current module comprises:

a first transistor operably coupled to produce the first current;

a second transistor operably coupled to produce the second current;

a first capacitor coupled between a gate of the first transistor and a first leg of the differential input signal; and

a second capacitor coupled between a gate of the second transistor and a second leg of the differential input signal.

23. An integrated circuit comprises:

digital circuitry operable to produce a plurality of data signals; and

a plurality of low voltage differential signaling (LVDS) drivers operably coupled to drive the plurality of data signals, wherein each of the plurality of LVDS drivers includes:

switchable current module operably coupled to produce a first current when a differential input signal is in a first state and to produce a second current when the differential input signal is in a second state, wherein the differential input signal is a corresponding one of the plurality of data signals;

source termination circuit operably coupled in parallel with a load;

transistor section operably coupled to receive the first and second currents from the switchable current module via at least one of the source termination circuit and the load, wherein the transistor section produces an LVDS output signal based on the first and second currents, the differential input signal, and the source termination circuit; and

load current source operably coupled to sink the first and second currents from the transistor section.

24. The integrated circuit of claim 23, wherein the source termination circuit comprises:

a first resistor and a second resistor coupled in series, wherein a common node of the first and second resistors corresponds to a common mode voltage of the LVDS output signal.

25. The integrated circuit of claim 24 further comprises:

an amplifier having a first input, a second input, and an output, wherein the first input is operably coupled to receive a reference voltage and the second input is operably coupled to the common node of the first and second resistors, wherein the output of the amplifier provides a control signal to the load current source to regulate the load current such that common mode voltage of the LVDS output is maintained at a desired voltage level.

26. The integrated circuit of claim 23, wherein the switchable current module comprises:

a first transistor operably coupled to produce the first current based on a first gating signal;

a second transistor operably coupled to produce the second current based on a second gating signal; and

gating module operably coupled to produce the first and second gating signals based on the differential input signal and a reference gate voltage.

27. The integrated circuit of claim 23 further comprises:

an adjustable current mirror module operably coupled to produce the reference gate voltage for the plurality of LVDS drivers;

wherein the gating module of each of the plurality of LVDS drivers includes:

a first switch operable to couple the reference gate voltage to a gate of the first transistor as the first gating signal when the differential input signal is in the first state; and

a second switch operable to couple the reference gate voltage to a gate of the second transistor as the second gating signal when the differential input signal is in the second state.

28. The integrated circuit of claim 27, wherein the switchable current module further comprises:

a first pull-up pull-down circuit operably coupled to the first transistor to actively turn on and turn off the first transistor in accordance with the first gating signal; and

a second pull-up pull-down circuit operably coupled to the second transistor to actively turn on and turn off the second transistor in accordance with the second gating signal.

29. The low power LVDS driver of claim 23, wherein the switchable current module comprises:

a first transistor operably coupled to produce the first current;

a second transistor operably coupled to produce the second current;

a first capacitor coupled between a gate of the first transistor and a first leg of the differential input signal; and

a second capacitor coupled between a gate of the second transistor and a second leg of the differential input signal.